Overview of the ATLAS Pixel Tracker

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Introduction: Motivations and Requirements

- Overall design concept

Module Design

- Sensors
- Front-end Electronics
- Integration into modules

Mechanical and Thermal Structures

Prototype Results

- Testbeam results from pixel assemblies

Summary and Status

ATLAS Inner Detector

Outermost system uses gas-filled 4mm straws

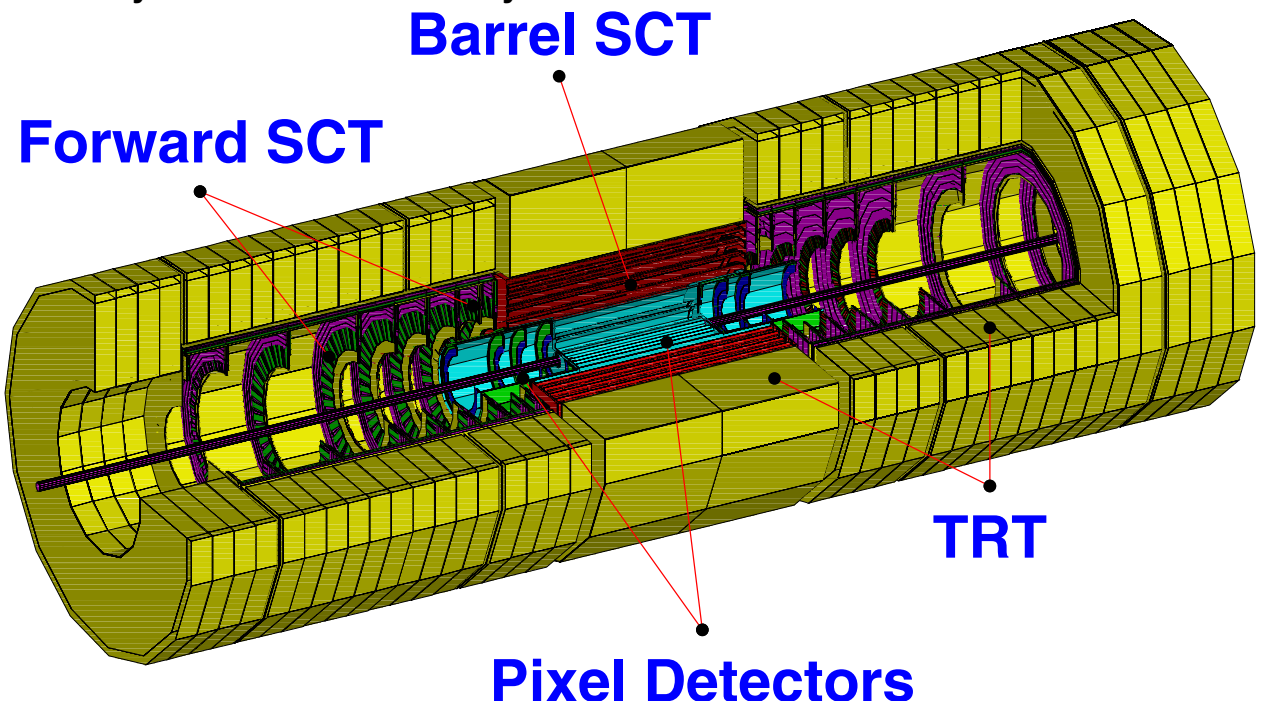
- There are 420K electronics channels, and a TR radiator supplies particle ID.

Intermediate radii contain a silicon strip tracker

- Four barrel layers and 9 disk layers contain 61 m^2 of silicon with 6.2M channels

Innermost system is pixel tracker

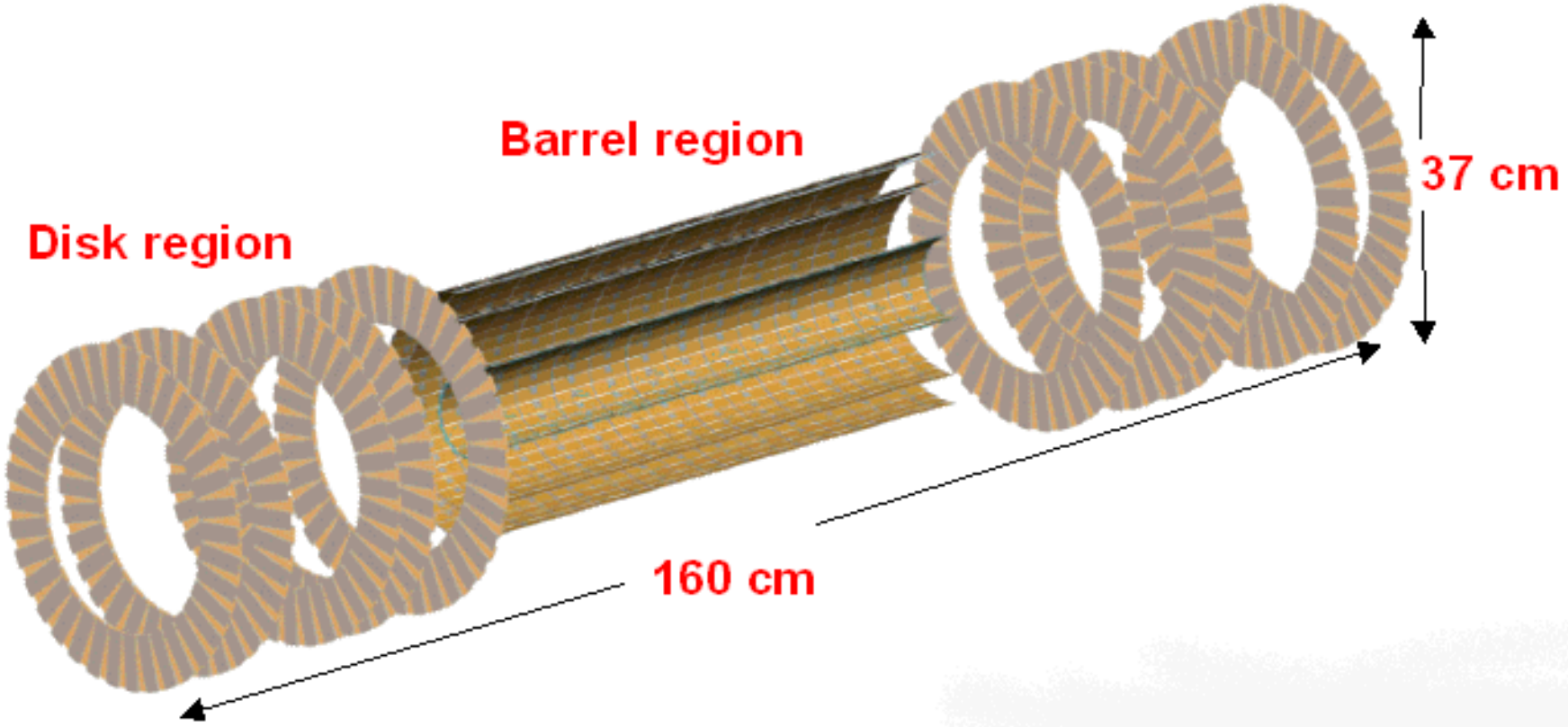
- Three barrel layers and 5 disk layers contain 2.3 m^2 of silicon and 100M channels



Pixel Tracking in ATLAS

Pixel concept uniquely addresses many vital tracking issues at the LHC:

- **Layout:** consists of 2 barrels at R=10 cm and 13 cm, plus 2 x 5 disks covering R=10-16 cm, and a small radius replacable barrel at R=4.5 cm to optimize impact parameter resolution, providing ≈ 2.3 m^2 total active area with ≈ 1.0 x 10^8 pixels arranged into ≈ 2200 pixel modules, providing three hits per track to η = 2.5



- **Radiation Hardness:** Principle issues are reduced signal size (low pixel capacitance reduces noise) and large leakage current (fine segmentation helps keep leakage below signal current). Signal size ($\propto$ depletion depth) limited by bias breakdown voltage, implying $\approx$ 10 cm is smallest radius for full-lifetime operation in ATLAS:

  $\rightarrow$ For a fluence of 10^{15}, expect $\approx$ 200μ depletion at 600V bias, and loss of $\approx$ 2 in signal for 250μ silicon detectors. Ability to operate with only about 10Ke signals gains a factor $\approx$ 5 in lifetime.

  $\rightarrow$ For this fluence, expect a leakage current of $\approx$ 25 nA for 50μ x 400μ pixels at -5 °C

- **Pattern Recognition:** Cope with $\approx$ 25 interactions/crossing at design luminosity

  $\rightarrow$ At design luminosity and 10 cm, the pixel occupancy is $\approx 10^{-4}$. It is 4-5 times worse at 4-5 cm

- **Parametric Performance:** Provide optimal impact parameter and z measurement with very low ambiguity

  $\rightarrow$ Binary readout should provide a point resolution of $\approx$ 14μ in rϕ and $\approx$ 90μ in z. Modest charge measurement could improve this by perhaps a factor of 2 for some angles.

- **Material:** Provide space points with a material budget per layer of < 2% X_0

  $\rightarrow$ Support structure must provide significant cooling, and accurate positioning from 20 °C to -15 °C

- **Coverage:** Need coverage over complete $|\eta| < 2.5$ tracking region

  $\rightarrow$ Combination of barrel and disk layers provide good uniformity for $\pm 2\sigma$ in z

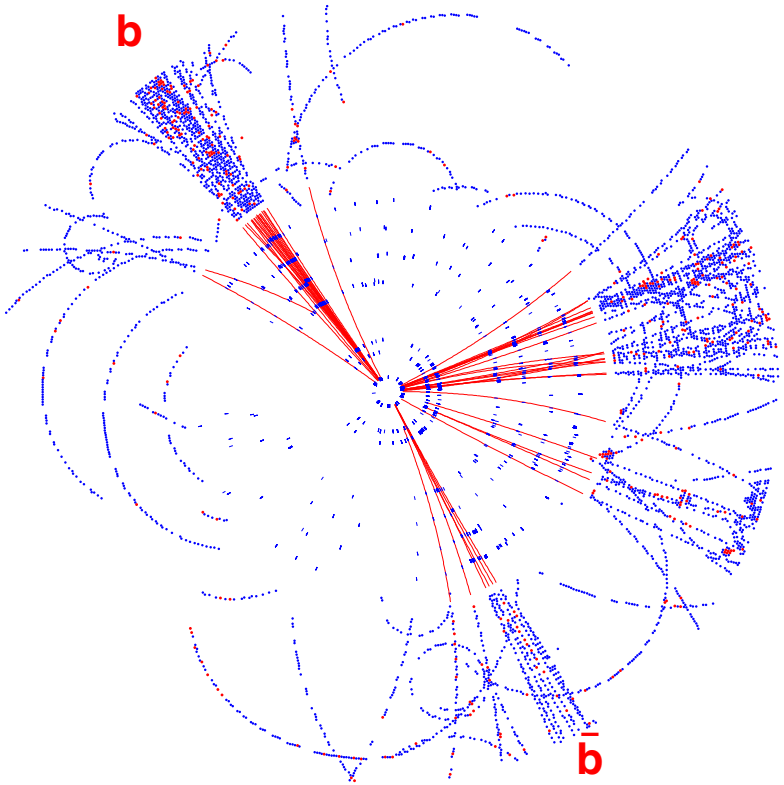
- **Trigger:** Space points and excellent resolution for rϕ and tanλ make these layers vital for the L2 tracking trigger

Pattern Recognition in ATLAS Inner Detector

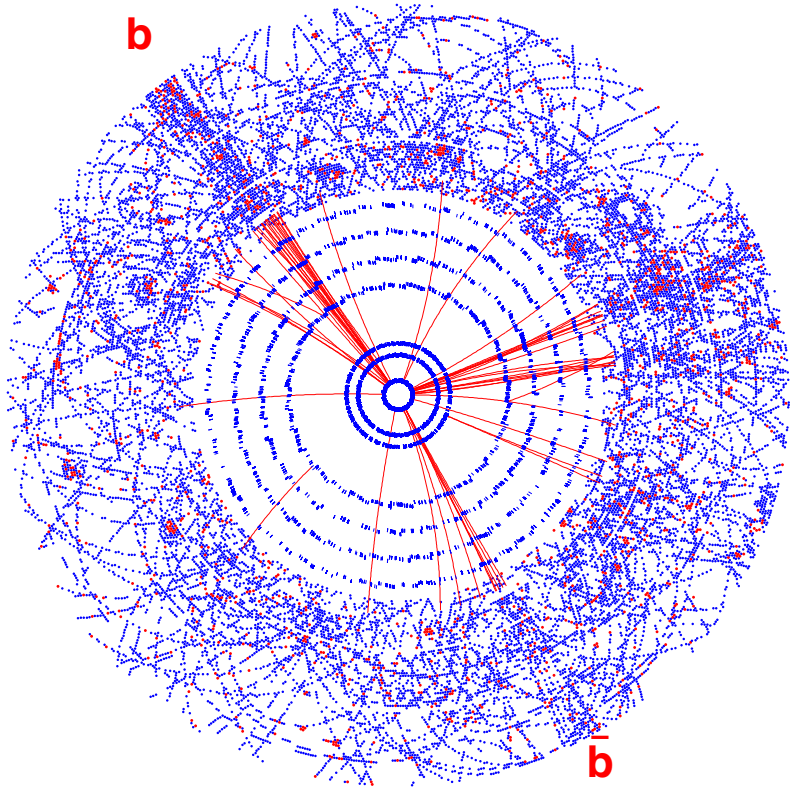
$H \rightarrow bb$ event at zero luminosity and at design luminosity:

- Vertexing and b-tagging will be challenging, and need pixel detectors !
  (Precision hits shown for $0 < \eta < 0.7$ only, TRT hits for $z > 0$ barrel only)

ATLAS Barrel Inner Detector
$H \rightarrow b\bar{b}$



ATLAS Barrel Inner Detector
$H \rightarrow b\bar{b}$

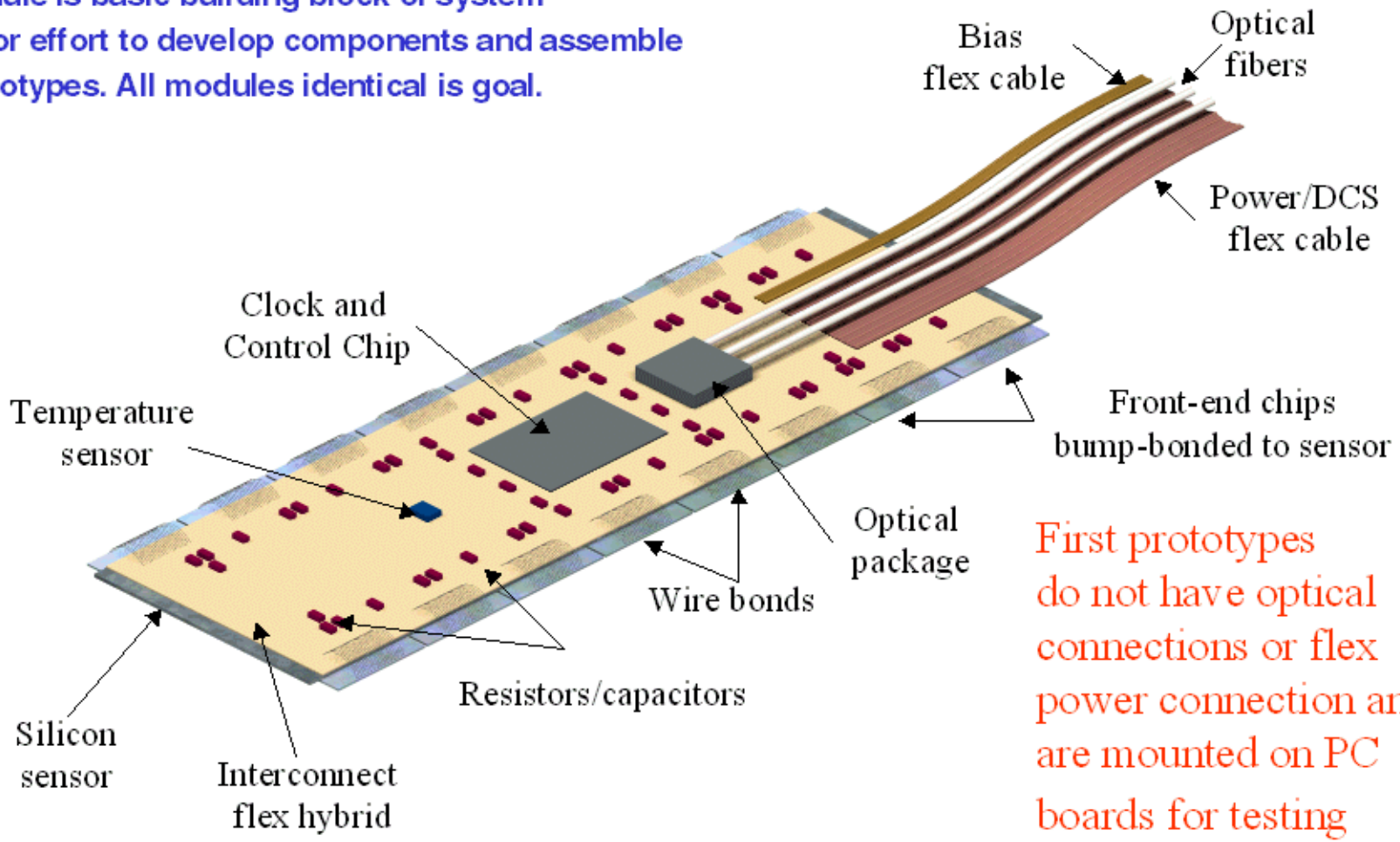


Basic Components of Pixel Tracker

Modules placed on a mechanical support/cooling structure:

- Silicon sensor with 16 FE chips, controller chip, power cable and opto-link

Module is basic building block of system
Major effort to develop components and assemble prototypes. All modules identical is goal.



First prototypes do not have optical connections or flex power connection and are mounted on PC boards for testing

Sensor Concepts

Basic requirement is operation after 10^{15} NIEL fluence:

- Requires partially depleted operation. Chosen n^+ pixels in n-bulk material as basic configuration (does require double-sided processing).
- Two isolation techniques have been studied for the n^+ pixel implants. First is conventional p-stop method. Second uses low-dose p implantation over the whole wafer (so-called p-spray). With p-spray technique, observe only bulk leakage in I/V curve after full dose (not true for p-stop), a bias grid can be used for wafer-scale testing, and no lithography between n^+ implants is needed.

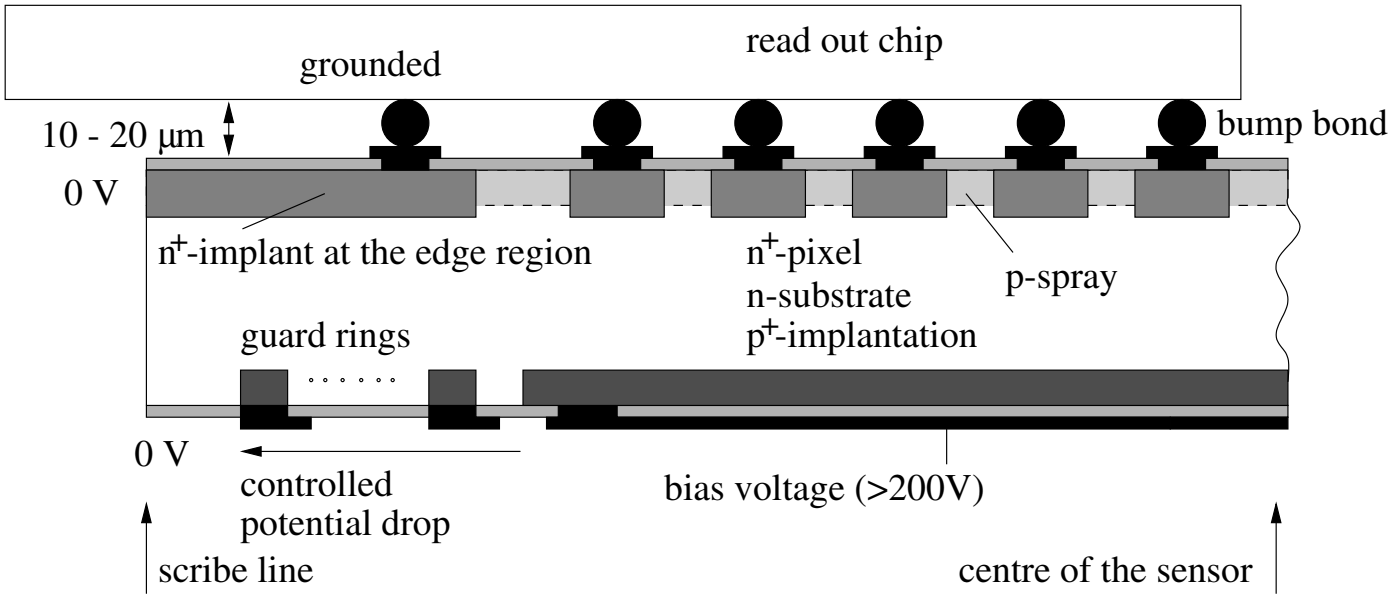
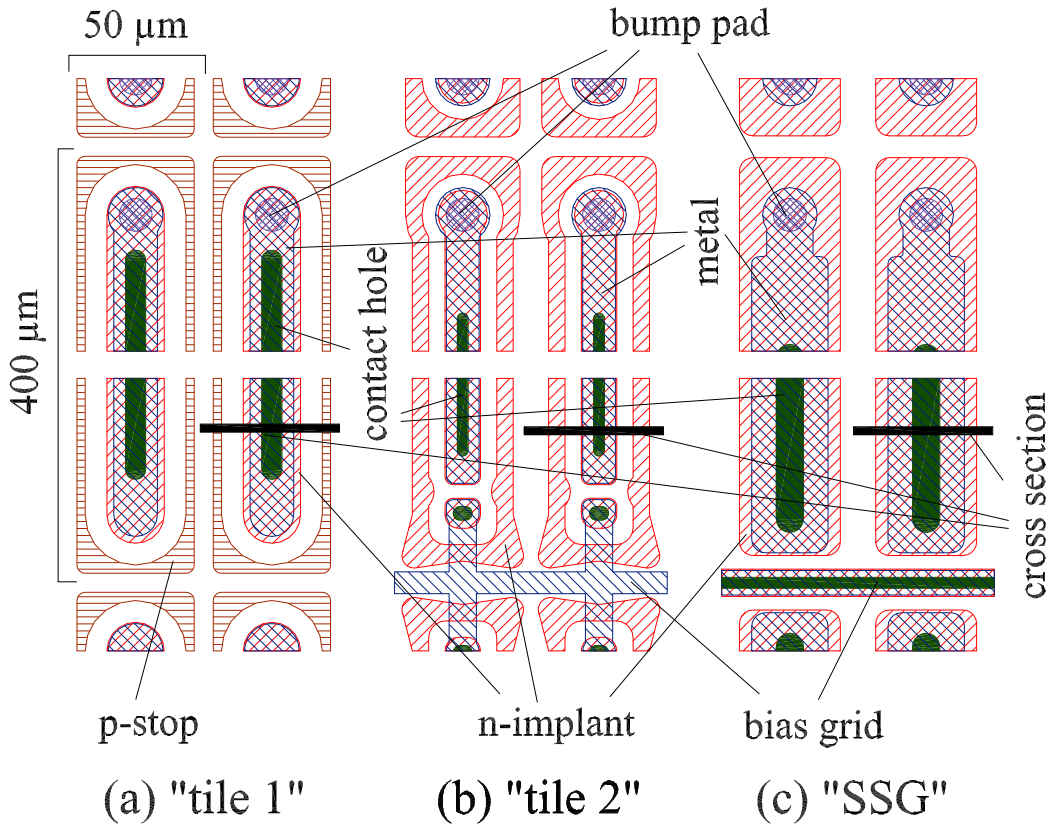


Diagram showing guard geometry near edges of module, designed to operate safely with bias voltages of beyond 700V.

Sensor Prototypes

Geometry of module:

- Design has an active region of 16.4 x 60.8mm, containing 46,080 pixels of 50μ x 400μ. The B-layer should use 61,440 50μ x 300μ pixels. The thickness will be 250μ in the outer layers, reduced to 200μ in the B-layer. An additional 1mm non-active region is used for the guard rings.
- Several designs were prototyped:



P-stop design had good charge collection and low capacitance, but had post-irradiation breakdown

Floating n-ring design had low capacitance but significant charge loss near ring.

Small gap design had higher capacitance, but otherwise excellent behavior.

Final Sensor Design

- Final design is based on small gap, and includes bias grid to allow testing (hold all pixel implants at ground for I/V characterization) and to keep unconnected pixels from floating to large potential in case of bump-bonding defects.
- Production wafer layout has 3 module tiles and many test structures in 4” wafer. Tendering complete, and preproduction order now in fabrication:

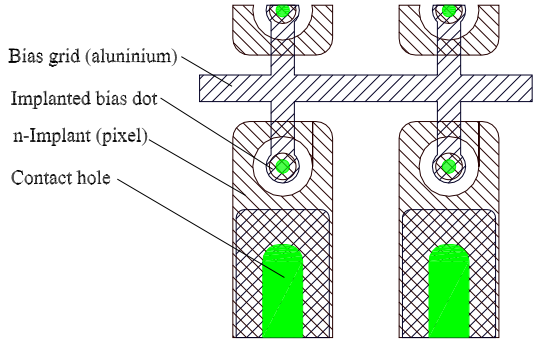
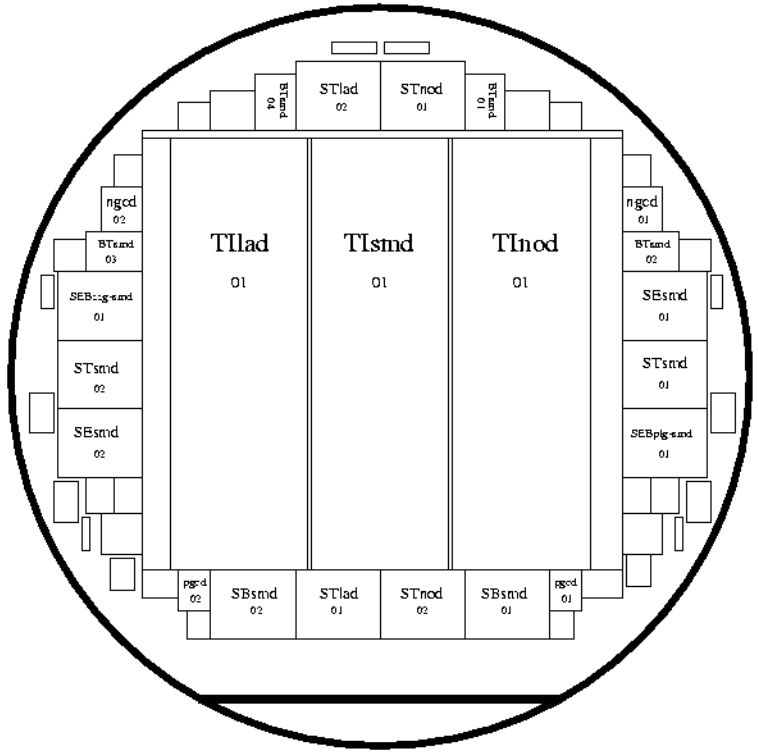
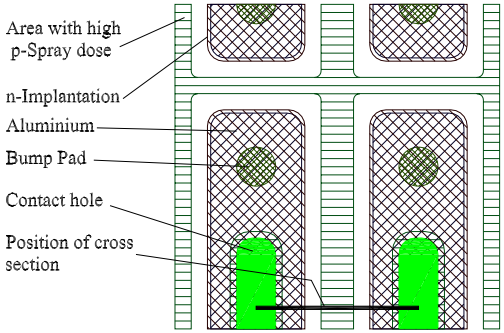
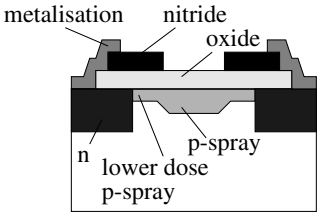


Fig. 10. Design detail of the bias grid in the second sensor prototype.







FE Electronics Concepts

System Design:

- **Pixel Array:** FE chip of 7.4 x 11.0mm die size with 7.2 x 8.0mm active area. The chip includes a serial command decoder, Clock, LVL1, and Sync timing inputs, and serial 40 Mbit/s data output. The set of hits associated with a particular crossing is “requested” by sending a LVL1 signal with the correct latency, and the FE chip then transmits the corresponding digital hits autonomously.
- **Module Controller:** Collects data from 16 FE chips and implements a silicon event builder. Performs basic integrity checks and formats data, also implements module level command and control. The 16 FE chips on a module connect in a star topology to the MCC to eliminate bottlenecks and increase fault tolerance.
- **Opto-link:** Multiplexed clock/control sent over 40 Mbit/s link to module, data is returned on one or two 80 Mbit/s data links. Transmitters are VCSELs, receivers are epitaxial Si PIN diodes. Basic link is 5x5x1.5mm package, and there are two additional small optolink chips with LVDS interfaces. The fibers are rad-hard silica core multi-mode fiber from Fujikura.
- **Power Distribution:** Significant ceramic decoupling used on module. Flex power tape used to reach services patchpanels on cryostat wall (1.5m) followed by Al round cable to later transition on back of calorimeter, then conventional cables to USA15 cavern.

Electronics Challenges and Requirements

Main challenges are in FE chips:

- Operate properly after total dose of 50 MRad (nominal ATLAS 10 year dose). Also cope with expected leakage currents from sensors of up to 50nA per pixel. For the B-layer, this corresponds to a lifetime of about 2 years at design luminosity.
- Operate with low noise occupancy (below 10^{-6} hits/pixel/crossing) at thresholds of about 3Ke with good enough timewalk to have an “in-time” threshold of about 4Ke (hit appears at output of discriminator within 20ns of expected time). This requires a small threshold dispersion (about 200e) and low noise (about 200e).
- Associate all hits uniquely with a given 25ns beam crossing. Contributions to this timing come from timewalk in the preamp/discriminator, digital timing on FE chip, clock distribution on module, and relative timing of different modules.
- Meet these specifications with an analog power budget of about 40μW/channel and a total power budget for the complete FE chip of about 250mW.

Electronics Prototypes

Several generations of prototypes have been built:

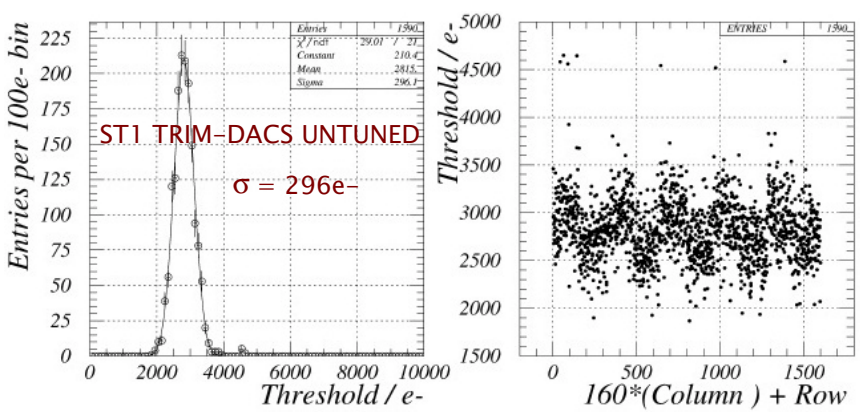
- First “proof of principle” chips were built in 96.
- First realistic prototypes were designed in two parallel efforts in 97/98, producing a rad-soft HP prototype (FE-B) and a rad-soft AMS prototype (FE-A/FE-C).
- Prototypes of critical elements made in both rad-hard processes (TEMIC DMILL and Honeywell SOI) to study performance and radiation hardness.
- Have just received first version of a common design DMILL chip (FE-D), and are working on common design Honeywell chip (FE-H). Vendor choice during 2000.

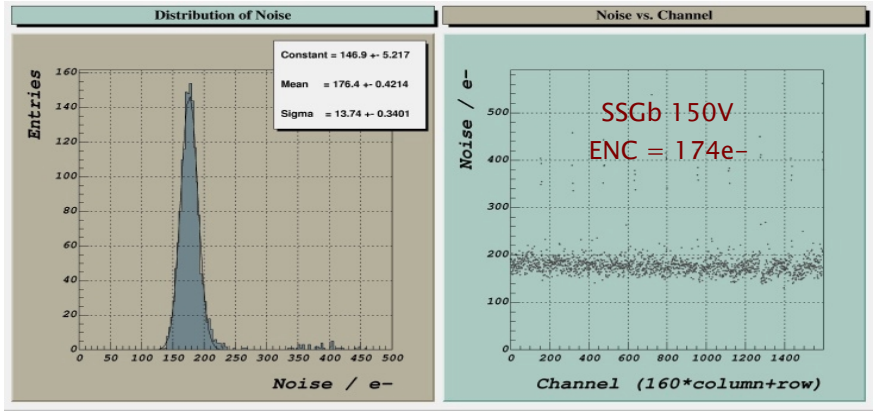
Features of final design:

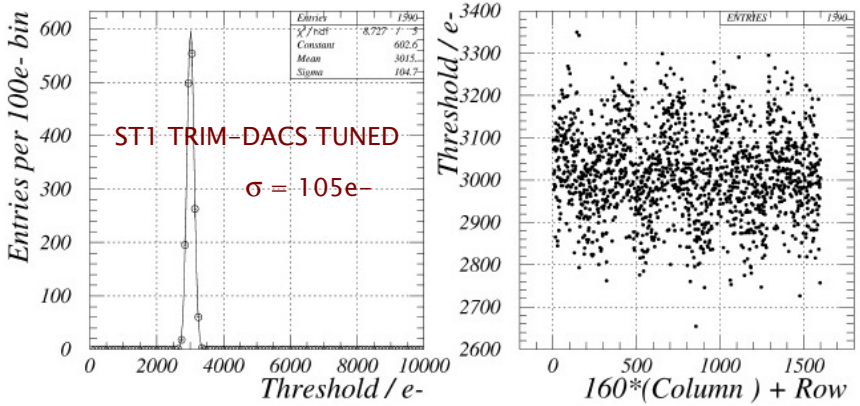
- Preamplifier provides excellent leakage current tolerance and relatively linear time-over-threshold (TOT) behavior via feedback bias adjustment.
- Discriminator is AC-coupled, and includes 3-bit trim DAC for threshold vernier.
- Readout architecture uses distributed 7-bit timestamp bus, and leading-edge plus trailing-edge latches in each pixel to define times of LE and TE.
- Asynchronous data push architecture used to get data into buffers at the bottom of the chip, where they are stored for the L1 latency, after which they are flagged for readout or deleted. Chip transmits Trigger/Row/Column/TOT for each hit.

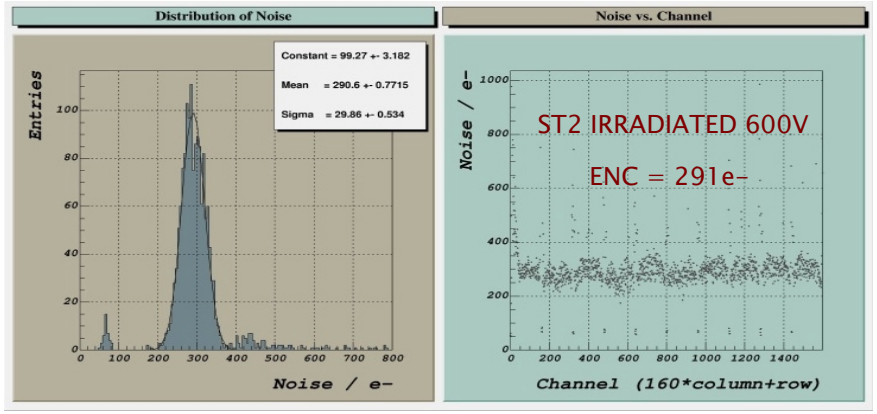
Lab Measurements

Examples of threshold and noise behavior in single chips:



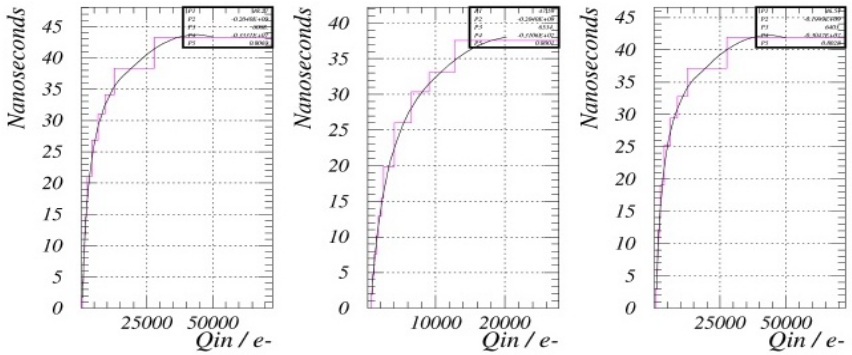


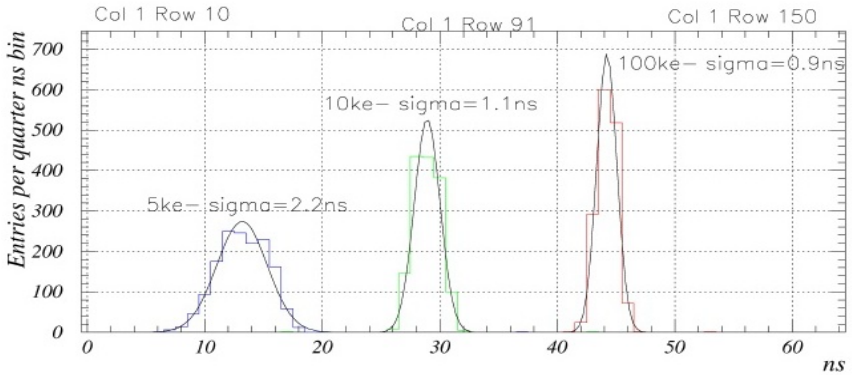




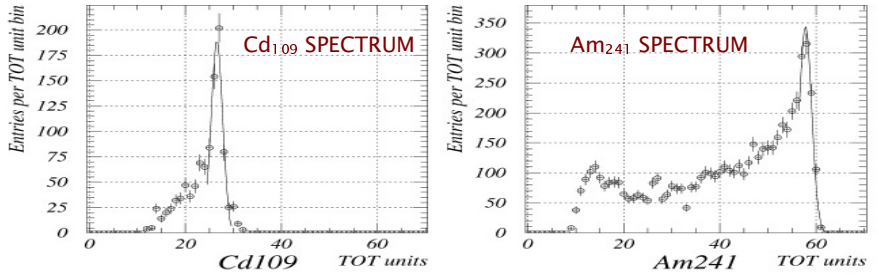
- Using individual Trim DACs, manage to achieve excellent dispersions.
- Measured noise is quite good, even for small-gap design pre-rad, and noise still remains acceptable after irradiation (reduced shaping time and parallel noise from leakage current itself both increase noise).

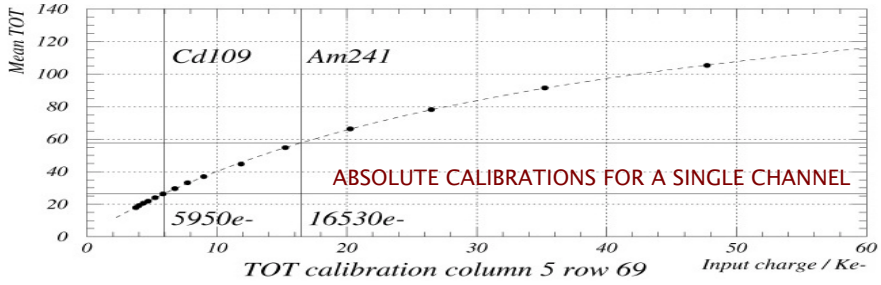
Examples of timing and charge measurements:

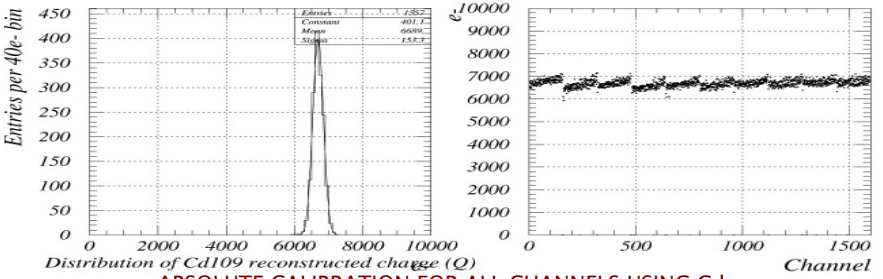




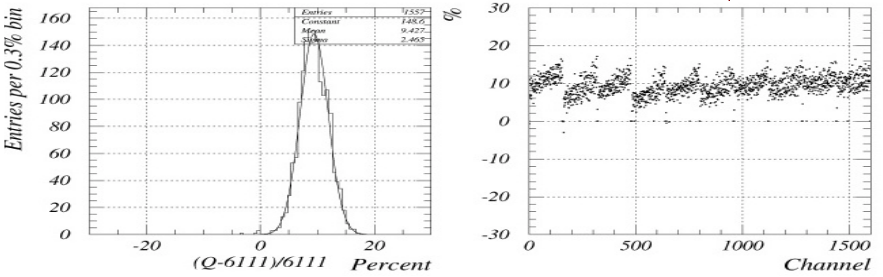
- Timing performance at large charge is excellent, and timewalk is acceptable.
- Charge measurement is high quality, but requires individual calibrations. Uniformity of internal calibration is good.







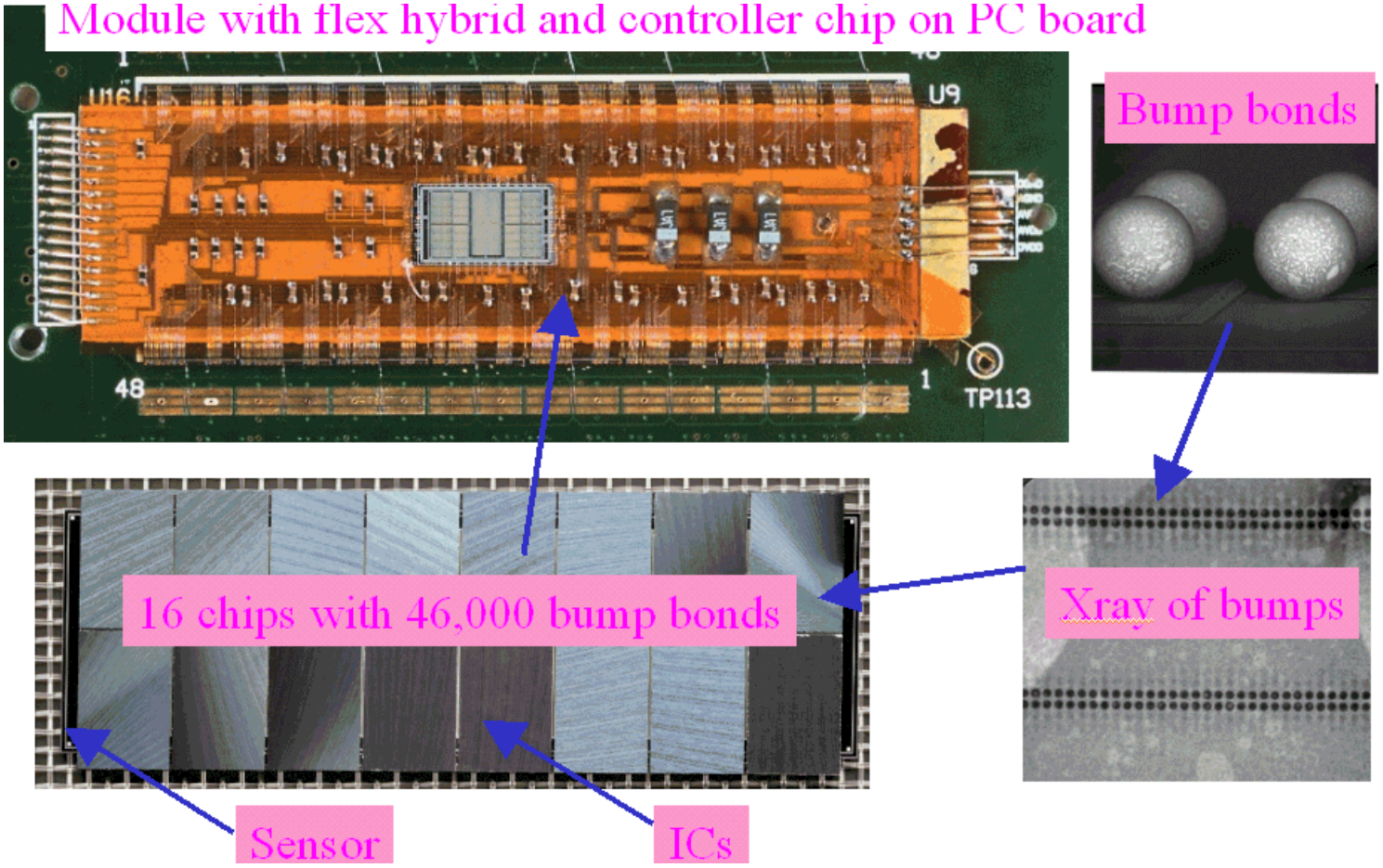
ABSOLUTE CALIBRATION FOR ALL CHANNELS USING Cd_1



Module Issues:

Major issue is interconnection:

- Connect 46K pixel implants on sensor to preamplifiers in FE electronics chip using bump-bonding technology (50μ pitch is not commercial standard !)
- Connect 16 FE chips with MCC chip and optolink components and power.



Bump Bonding:

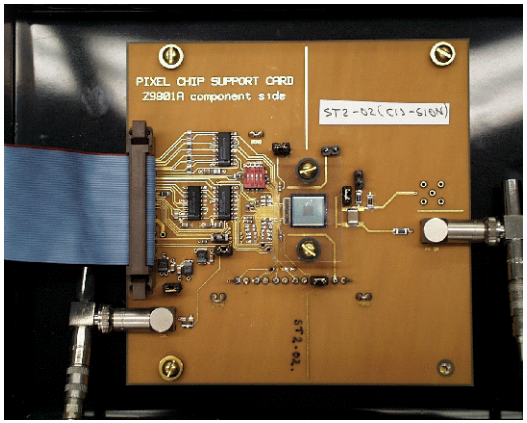
- Have worked with many vendors over the years (Rockwell/Boeing, Seiko, MCNC, DTO, LETI/Tronics), none of which are candidates for production at this time because they are no longer willing to provide 50μ pitch bump-bonding.
- Presently concentrating on three vendors: IZM (Berlin) providing solder bumps, Alenia (Rome) providing Indium bumps, and Sofradir (Grenoble) providing reflow Indium bumps. They are likely to be the only candidates for production bumping.
- Our experience has been that these firms are capable of providing 50μ pitch bumps with low resistance and high yield (no more than 10^{-4} bump defect rate). Our experience with them is still small scale (a total of only about 15 modules between all vendors), and technical issues remain. The next year will be critical to deal with these issues and ramp up towards production work.
- Very limited experience with thinned electronics wafers. For production, the wafers should be thinned, almost certainly after bumping, to 150μ - 300μ, depending on yield issues. Several wafers with bumps are now being thinned, and we will have much more experience soon.

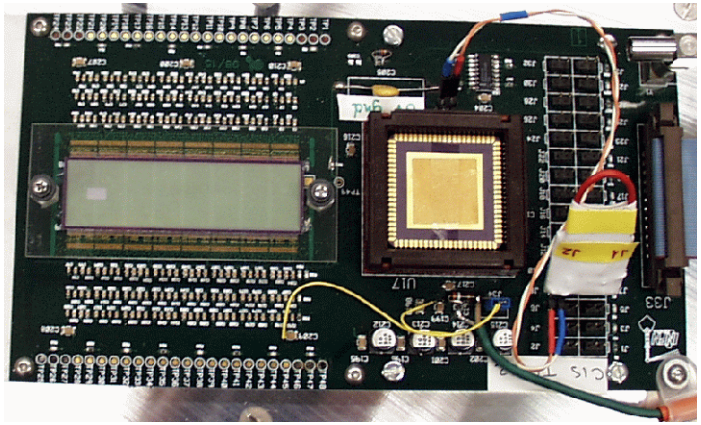
Module Integration:

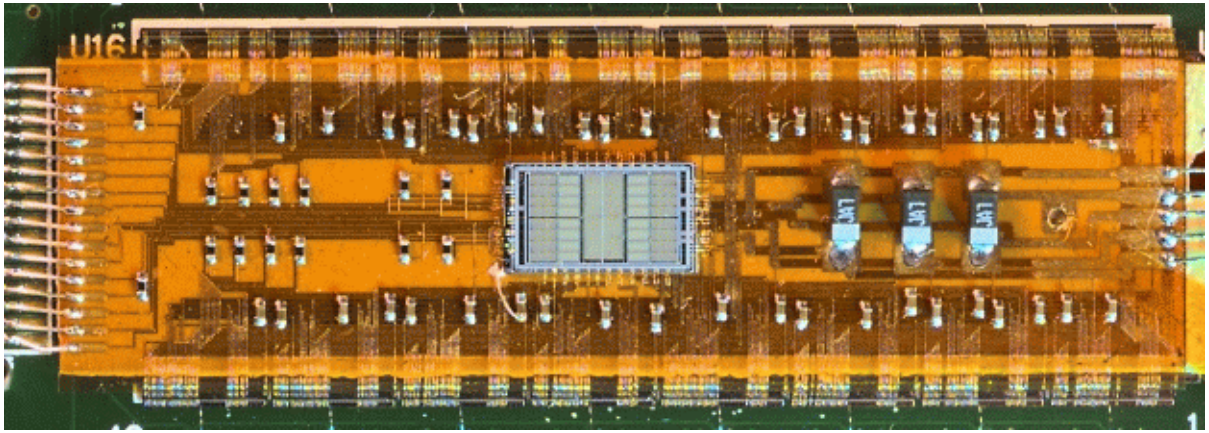
- Baseline for outer layers is Kapton Flex hybrid. This is a double-sided 25-50μ thick Kapton Flex with coverlayer on both sides, which is glued to the sensor surface. All passive and active components are mounted on it. Have successfully fabricated parts with CERN shop, and 1-2 commercial vendors look promising.
- Baseline scheme for B-layer is MCM-D, with interconnections deposited directly on sensor wafers. In this case, the sensor is larger and becomes a substrate for the MCM-D interconnections, with a “balcony” on one end of the module for the MCC, optolink, and all passive components. This integration technique eliminates all wire-bonds, but requires more material and is technically much more demanding. Presently have had one working prototype from a single vendor (IZM). Further work is continuing, with Flex as a backup solution.
- In general, integration of the module is a very challenging electrical, mechanical, and thermal problem. The hybrid pixel design couples the electronics and sensor very tightly (5-20μ separation), and achieving low noise operation is challenging. Each module should dissipate a nominal power of 5W, with a worst case spec of 8-10W. Transfering this heat into a small low mass cooling tube requires innovative materials. The large temperature range of +25C to -15C requires carefully matching of CTE, and the use of low modulus adhesive techniques. Everything must also survive radiation doses of 50 MRad.
- Not all of these issues are resolved at the present time.

Module Prototyping:

- Built many “single chip” devices using smaller sensors for small-scale studies. Some studies were done with irradiated sensors and rad-soft electronics.
- Built about 10 modules with IZM solder bumps, several as “bare” modules with interconnections on PC board, several as “Flex” modules, others as “MCM-D” modules. Some, but not all, of these modules work very well.

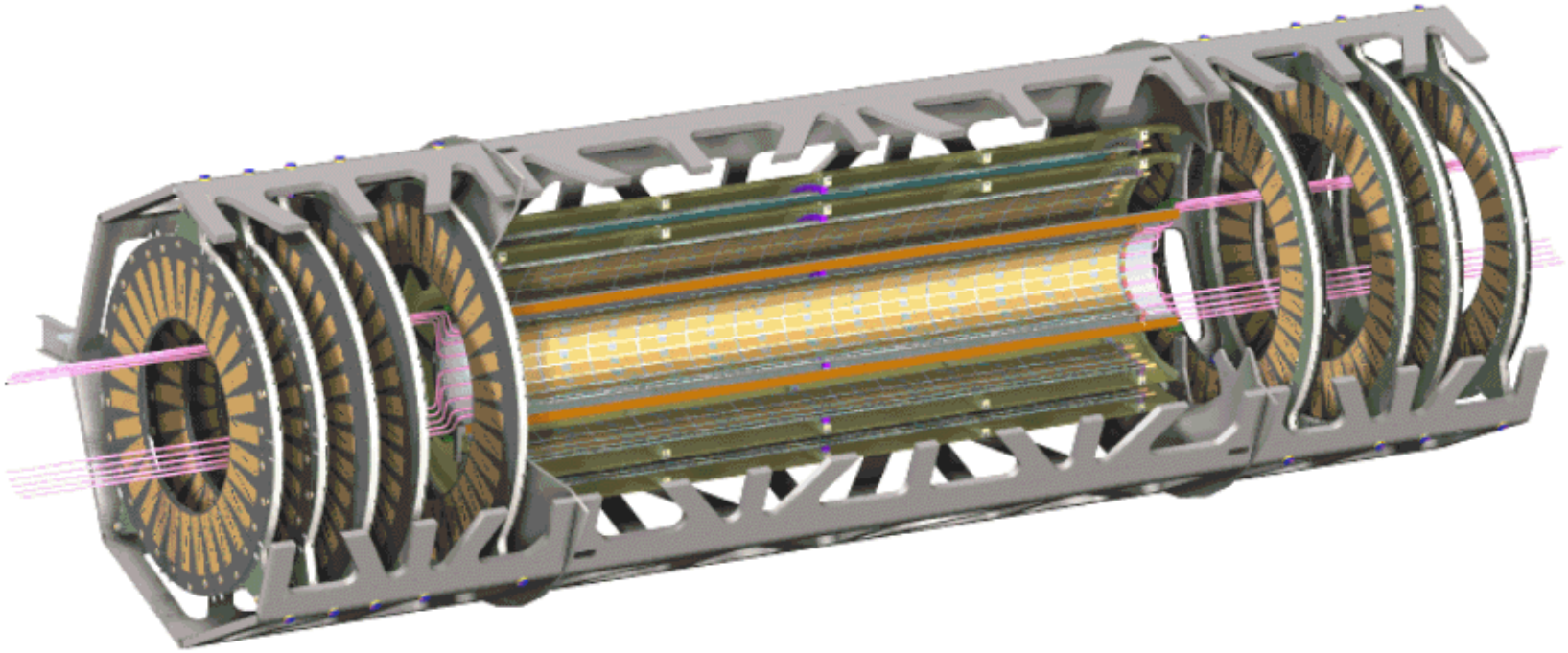






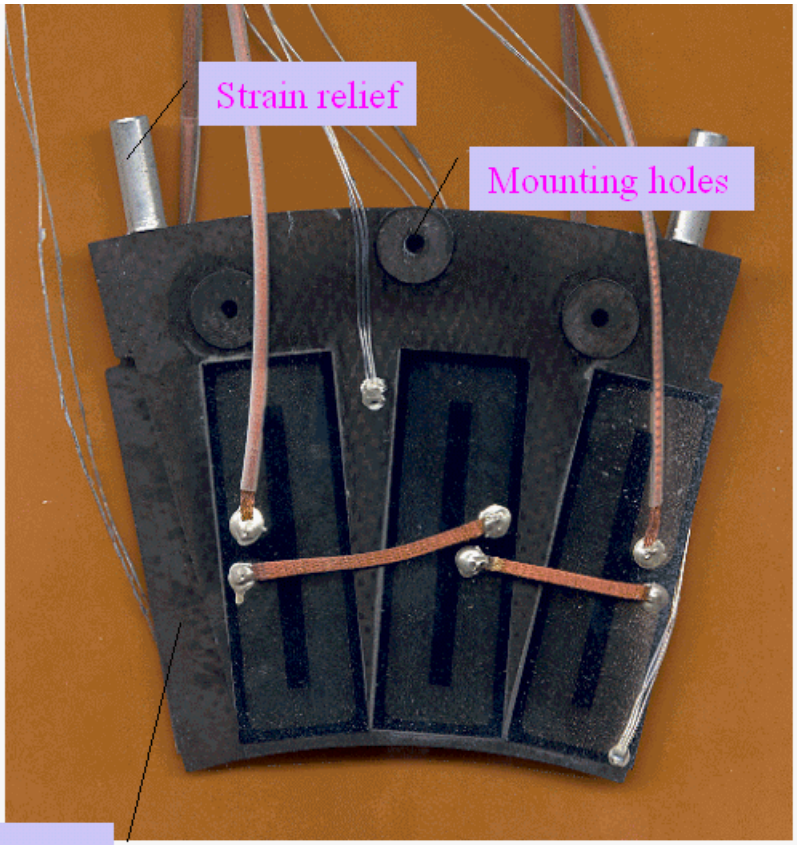
Mechanics and Cooling

- High power density and large temperature range in a high precision low mass structure present unique challenges.
- Local support structures are based on carbon-carbon material with carbon (or possibly Al) cooling channels to achieve good conductivity in all directions and very low CTE. Modules are attached with high thermal conductivity adhesive to barrel staves and disk sectors.
- Global support uses panels with very thin carbon-fiber facings and carbon-fiber honeycomb material to build up a very strong and low mass structure.



- Cooling system uses flurocarbons (most likely C3F8) injected through small orifices in liquid form. Phase change into gas provides cooling capacity, but requires relatively large exit piping and complex feedback system to control temperature of structures. Small scale tests OK, but system tests are critical.
- Many prototypes exist for local structures (staves and sectors), including detailed thermal and structural measurements (displacements under temperature cycling). First prototypes for global support just now being built.

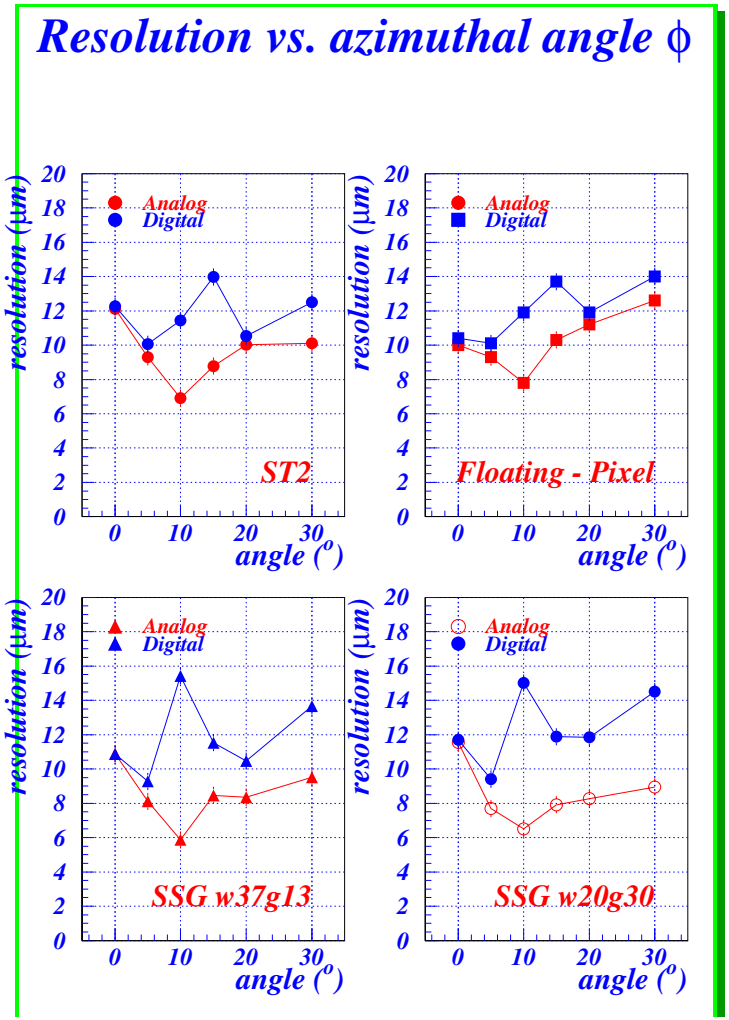
Leak tight carbon tube flocked with high thermal conductivity fibers.

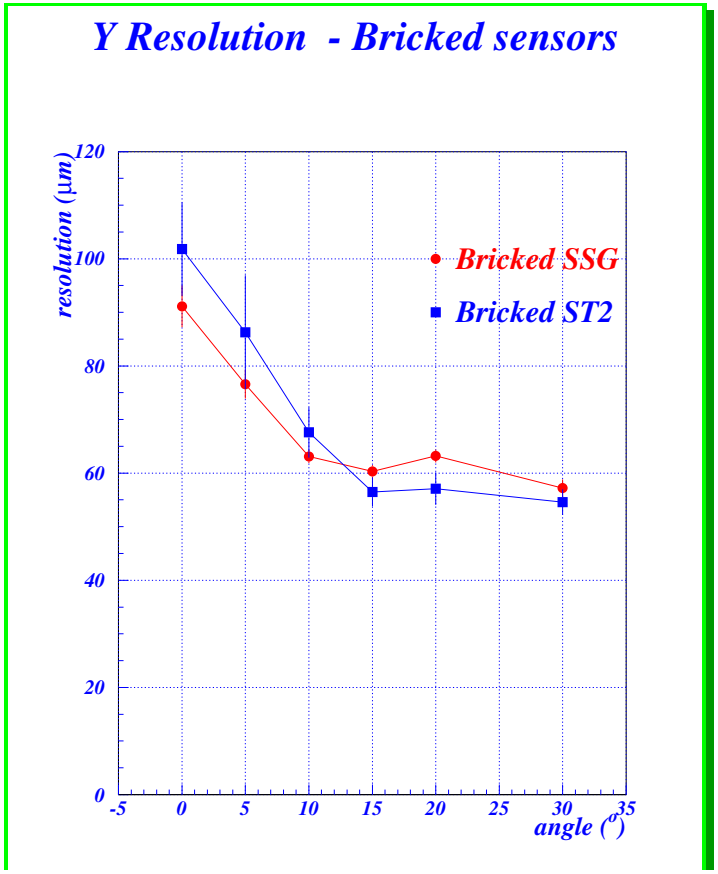


Electronics/Sensor Prototype Results

Measure resolution versus incident track angle:

- Compare digital (binary) and analog algorithms for different sensor types, and also compare effect of "bricking" (half-pixel stagger) in long direction of pixel:



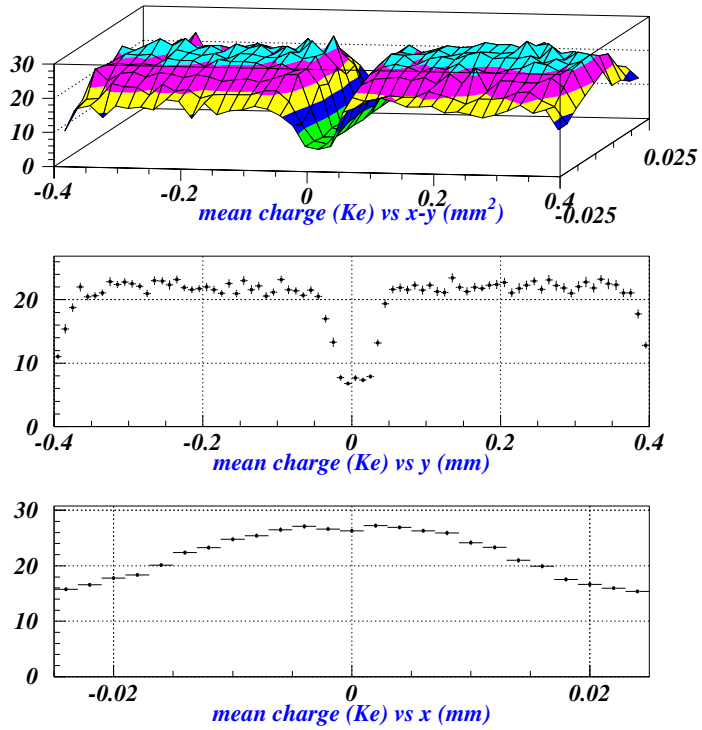


Could achieve perhaps 8-10μ in narrow and 60-80μ in wide direction for best case in barrel

Measure charge collection versus track location in pixel:

- Original n-ring design has serious charge loss problems, while new small-gap design is much better, with only small loss at bias dot location:

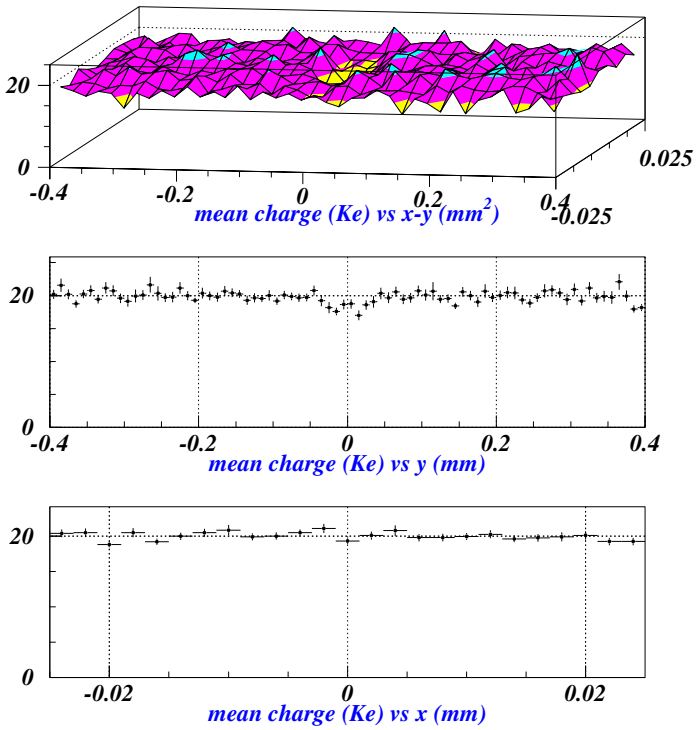
Tile 2 Design Threshold 2 Ke



large loss (0.7) near the grid
loss located ± 30 μm around the grid
losses at the pixel edges

Design 1.b:

- *p-spray insulation*
- *no floating atoll*
- *modified bias grid*



Measure efficiency as a function of track arrival time:

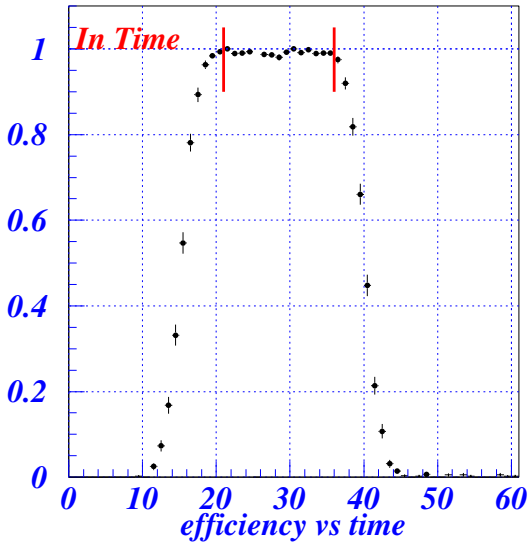
- Behavior of new design (pre-rad) is excellent, and behavior of old design (post-rad) is very good, provided that poor charge collection regions are removed:

Efficiency 'In Time'

Detector Tile 2 new design (with bias grid)

not Irradiated - Thr. 3 Ke

efficiency 99.1		***Losses***	***0.9***
1 hit	***81.8***	***0 hits***	***0.4***
2 hits	***15.6***	***not matched***	***0.1***
>2 hits	***1.7***	***not in time***	***0.4***

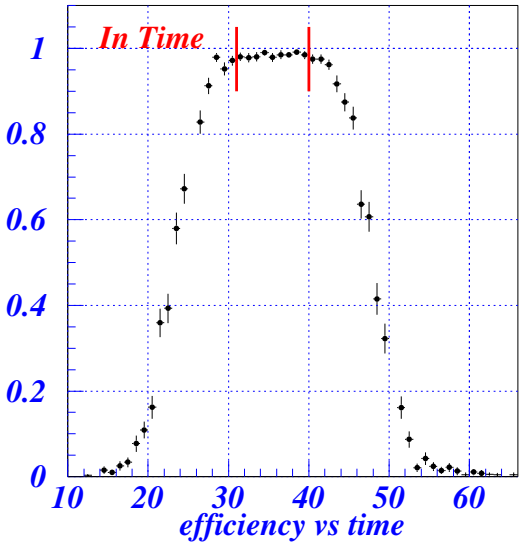


Efficiency 'In Time'

Detector Tile 2 - Irradiated V_{bias} = 600 V

Fluence 10^{15} n/cm^2 - Thr. 3 Ke

efficiency 98.4		***Losses***	***1.6***
1 hit	***94.2***	***0 hits***	***0.4***
2 hits	***3.1***	***not matched***	***0.0***
>2 hits	***1.1***	***not in time***	***1.2***



|xloc| < 0.01

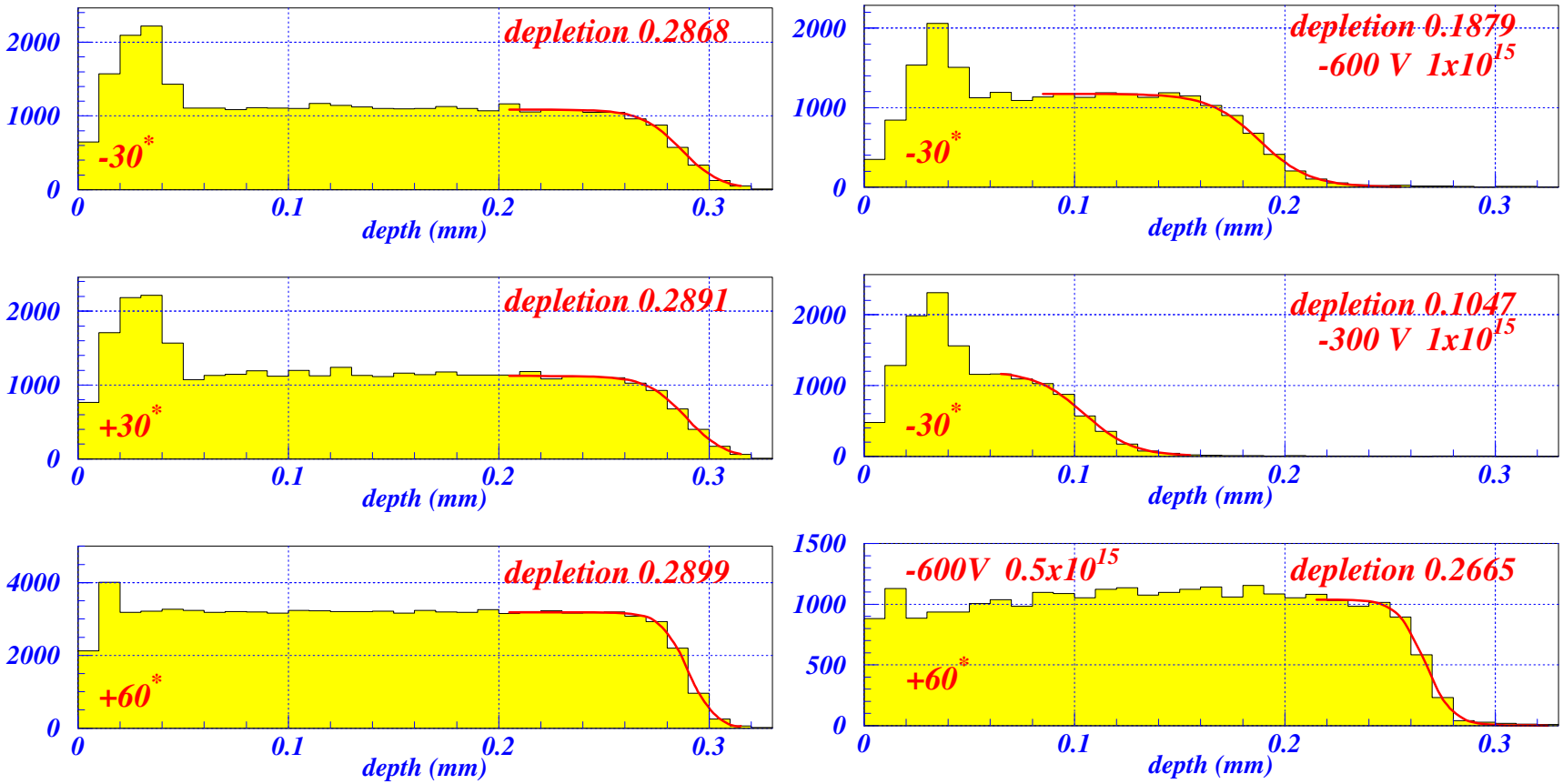
|yloc| < 0.15

Measure depletion depth in sensors:

- Look at cluster width for highly inclined tracks and use this to measure uniformity and depth of charge collection inside of sensor:

Not irradiated - depletion depth

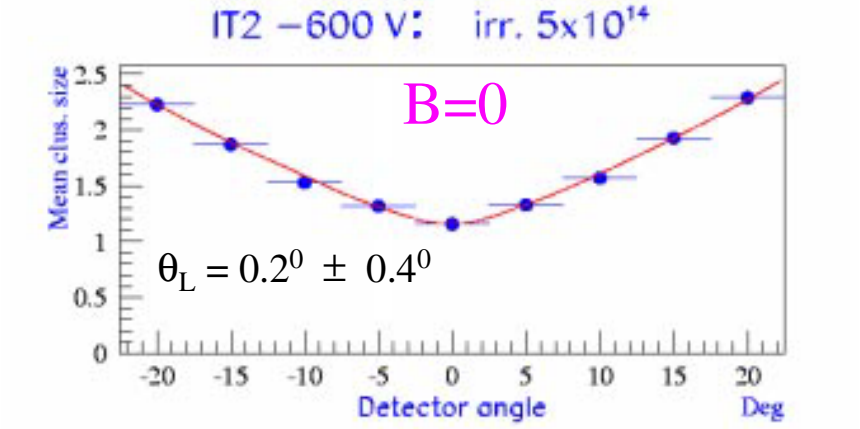
Irradiated - depletion depth



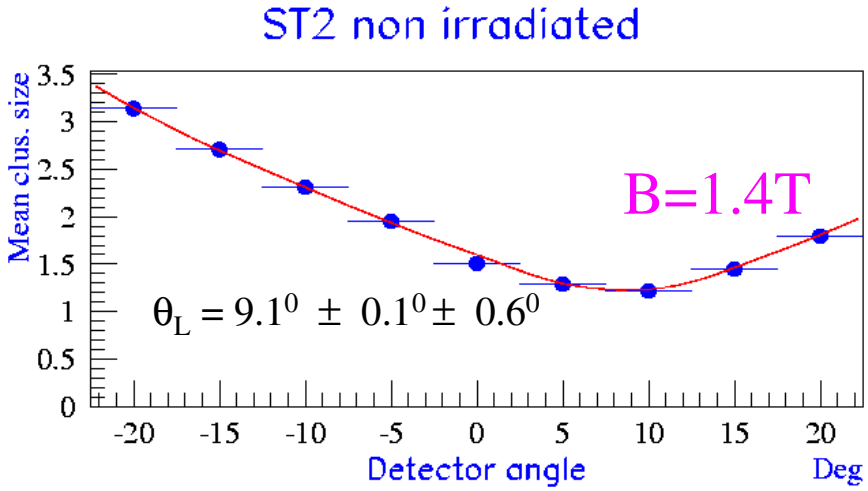
- Pre-rad result agrees with 280μ thickness. At 600V bias, lose full depletion at about half the lifetime dose, and still collect from about 180μ after lifetime dose.

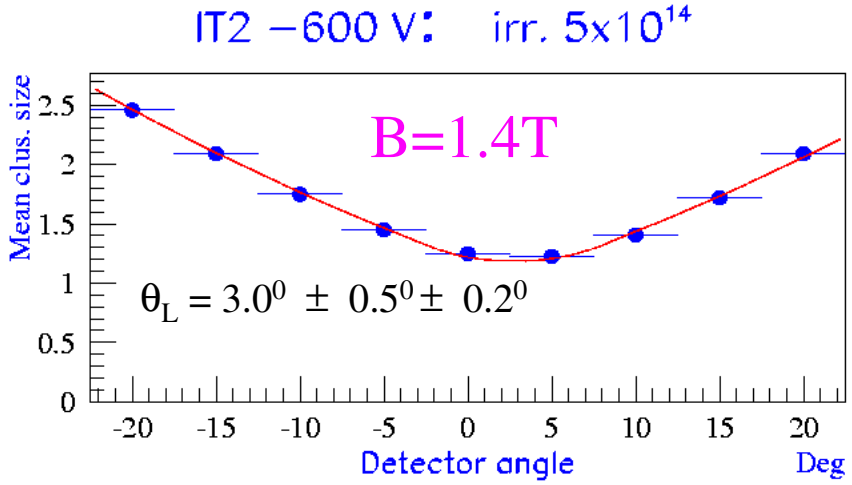
Measure Lorentz angle in sensors:

- Use cluster width versus angle of incidence, doing parallel runs with and without magnetic field, to extract angle at which cluster width is minimum:



not irradiated	$9.1^0 \pm 0.1^0 \pm 0.6^0$
dose $5\ 10^{14}$ n/cm²	$3.0^0 \pm 0.5^0 \pm 0.2^0$
dose 10^{15} n/cm²	$3.2^0 \pm 1.2^0 \pm 0.5^0$





- Significant reduction after irradiation due to reduced mobility at higher E fields ?

Summary

- Realistic prototypes exist for electronics and sensors. They meet essentially all of our design goals. An extensive testbeam effort has been critical in assessing the performance of these ingredients. Major further milestone is radiation hard versions of electronics.
- A small number of modules have been built, and some of them meet most requirements. However, much more experience is required building modules and optimizing their assembly into a production process. We must also demonstrate that we have mastered all of the electrical/mechanical/thermal issues at the same time.
- Relatively mature designs exist for the local and global mechanical supports and cooling structures. Many prototypes have already been built and measured. The mechanics is aggressive, but most major technical issues have been dealt with. System tests will be the next critical milestone for cooling.
- Some technical issues, as well as an extraordinary amount of work still remain. Nevertheless, we are largely where we need to be to begin production in 2001 and deliver a complete pixel tracker in 2003 to ATLAS for commissioning.